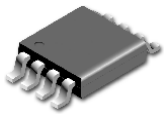
DDR Termination Regulator TJ2996

FEATURES

- Source and sink current
- Low output voltage offset
- No external resistors required
- Linear topology
- Suspend to Ram (STR) functionality
- Low external component count
- Thermal Shutdown
- Available in SOP8, SOP8-PP Packages

SOP8 / SOP8-PP PKG



APPLICATION

- DDR-I, DDR-II and DDR-III Termination Voltage
- SSTL-2 and SSTL-3 Termination
- HSTL Termination

ORDERING INFORMATION

Device	Package
TJ2996D	SOP8
TJ2996DP	SOP8-PP

DESCRIPSION

The TJ2996 linear regulator is designed to meet the JEDEC SSTL-2 and SSTL-3 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The TJ2996 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DIMMs. An additional feature found on the TJ2996 is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the V_{TT} output will tri-state providing a high impedance output, but, V_{REF} will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage to GND	PV_{IN} AV_{IN} V_{DDQ}	-0.3 -0.3 -0.3	6.0 6.0 6.0	V
Lead Temperature (Soldering, 10 sec)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	-65	150	℃
Operating Junction Temperature Range	T_{JOPR}	-40	125	℃

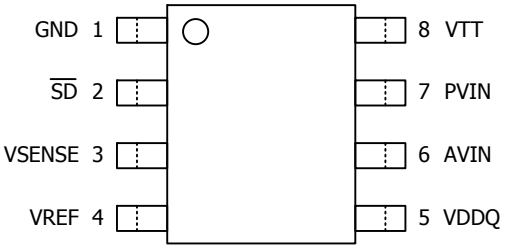
Recommended Operation Range

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
AV_{IN} to GND	AV_{IN}	2.3	5.5	V
PV_{IN} & SDV_{IN} to GND	PV_{IN} & SD Input	0	AV_{IN}	V

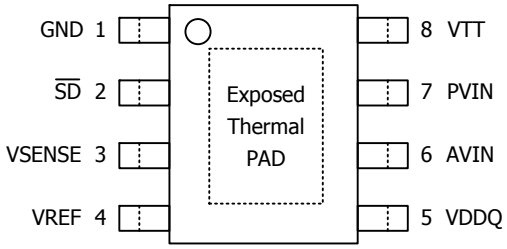
Ordering Information

Package	Order No.	Description	Package Marking	Supplied As
SOP8	TJ2996D	DDR Termination Regulator	TJ2996	Reel
SOP8-PP	TJ2996DP	DDR Termination Regulator	TJ2996	Reel

PIN CONFIGURATION



SOP8

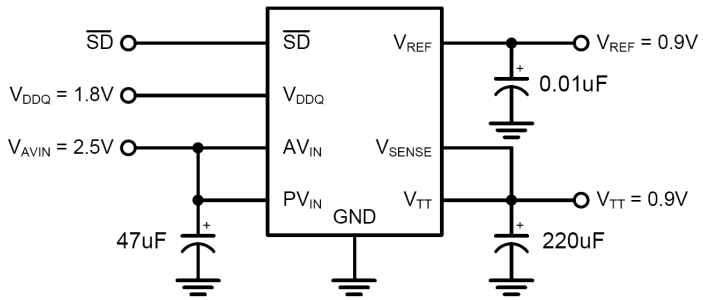


SOP8-PP

PIN DESCRIPTION

Pin No.	Pin Name	Pin Function
1	GND	Ground
2	$\overline{SD}$	Enable
3	VSENSE	Feedback Pin for Regulating V_{TT}
4	VREF	Buffered Internal Reference Voltage of $V_{DDQ}/2$
5	VDDQ	Input for Internal Reference Equal to $V_{DDQ}/2$
6	AVIN	Analog Input Pin
7	PVIN	Power Input Pin
8	VTT	Output Voltage for Connection to Termination Resistors
	Exposed Thermal PAD	Exposed Thermal Connection. Connect to Ground. (SOP8-PP Only)

TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS (1)

Specifications with standard typeface are for T_J = 25˚. Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V (1), (2), (3), (4) for DDR Ⅰ, AVIN = 2.5V, PVIN = VDDQ = 1.8V(1), (2), (3) for DDRⅡ. AVIN = 2.5V, PVIN = VDDQ = 1.5V(1), (2), (3) for DDRⅢ.

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{REF} Voltage	V_{REF}	V_{DDQ} = 2.5V	1.21	1.25	1.29	V
V_{REF} Voltage	V_{REF}	V_{DDQ} = 1.8V	0.86	0.90	0.94	V
V_{REF} Voltage	V_{REF}	V_{DDQ} = 1.5V	0.71	0.75	0.79	V
V_{TT} Output Voltage	V_{TT}	I_{OUT} = 0 A V_{DDQ} = 2.5V I_{OUT} = ± 1.5 A (7) V_{DDQ} = 2.5V	1.21 1.21	1.25 1.25	1.29 1.29	V
V_{TT} Output Voltage	V_{TT}	I_{OUT} = 0 A V_{DDQ} = 1.8V I_{OUT} = ± 0.9 A (7) V_{DDQ} = 1.8V	0.86 0.86	0.90 0.90	0.94 0.94	V
V_{TT} Output Voltage	V_{TT}	I_{OUT} = 0 A V_{DDQ} = 1.5V I_{OUT} = ± 0.5 A (7) V_{DDQ} = 1.5V	0.71 0.71	0.75 0.75	0.79 0.79	V
V_{TT} Output Voltage Offset	V_{OSVTT}	I_{OUT} = 0 A I_{OUT} = ± 0.5 A (7) I_{OUT} = ± 0.9 A (7) I_{OUT} = ± 1.5 A (7)	-40 -40 -40 -40	0 0 0 0	40 40 40 40	mV
Quiescent Current (5)	I_Q	I_{OUT} = 0A	-	250	2000	uA
V_{DDQ} Input Impedance	Z_{VDDQ}		-	100	-	kΩ
Quiescent Current in Shutdown(5)	I_{SD}	$\overline{SD}$ = 0V		200	2000	uA
Shutdown Leakage Current	I_{Q_SD}	$\overline{SD}$ = 0V		0.1	0.5	uA
Minimum Enable High Level	V_{IH}		1.9 (8)	-	-	V
Maximum Enable Low Level	V_{IL}		-	-	0.6	V
V_{TT} Leakage Current in Shutdown	I_V	$\overline{SD}$ = 0V, V_{TT} = 1.25V		1	10	uA
V_{SENSE} Input Current	I_{SENSE}		-	-	0.1	uA
Thermal Shutdown(6)	T_{SD}		-	165	-	℃

Note 1. Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2. At elevated temperatures, devices must be derated based on thermal resistance. The device in the SOP8 package must be derated at Θ_{JA} = 165° C/W junction to ambient with no heat sink.

Note 3. Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation.

Note 4. V_{IN} is defined as $V_{IN} = AV_{IN} = PV_{IN}$

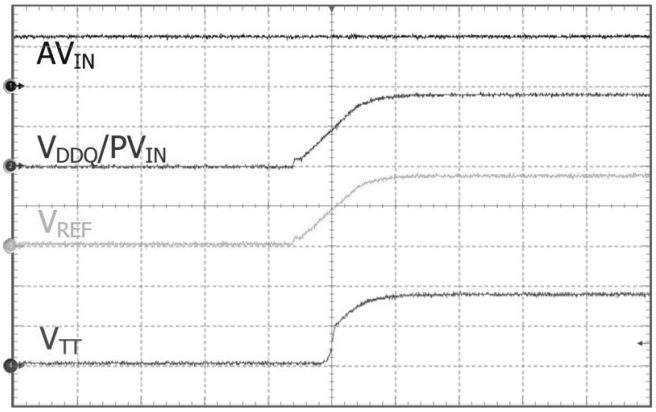
Note 5. Quiescent current defined as the current flow into AV_{IN}.

Note 6. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

Note 7. V_{TT} load regulation is tested by using a 10 ms current pulse and measuring V_{TT}.

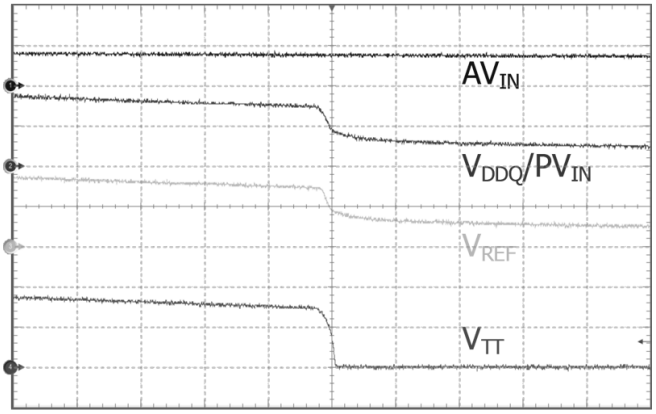
Note 8. In the case of AV_{IN} > 2.5V, minimum enable high level is AV_{IN} * 0.7.

TYPICAL OPERATING CHARACTERISTICS



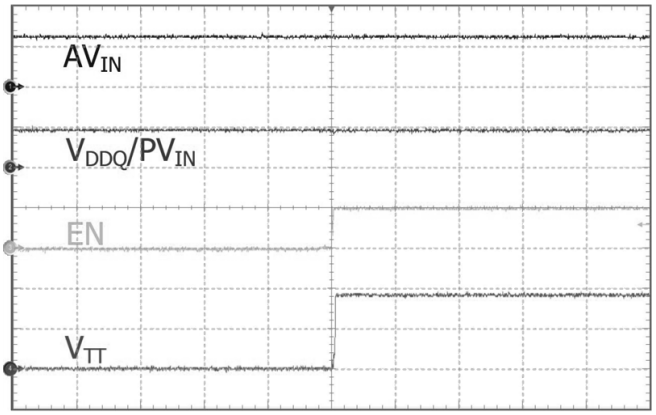
AVIN : 2.0V/div, VDDQ/PVIN : 1.0V/div, VREF : 500mV/div, VTT : 500mV/div, Time : 10ms/div

Start Up



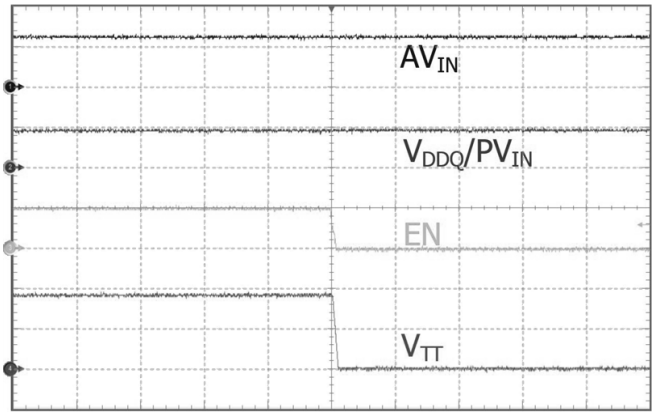
AVIN : 2.0V/div, VDDQ/PVIN : 1.0V/div, VREF : 500mV/div, VTT : 500mV/div, Time : 10ms/div

Shut Down



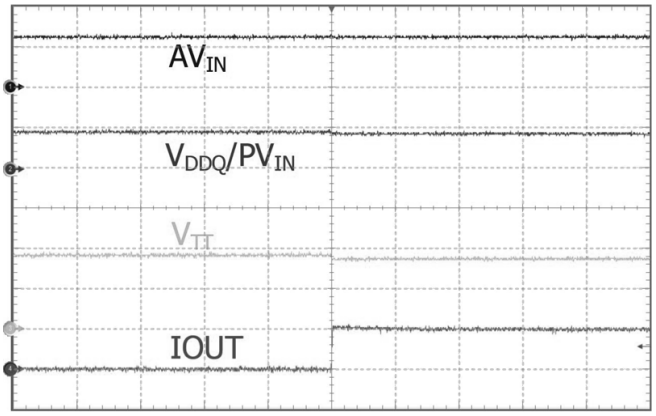
AVIN : 2.0V/div, VDDQ/PVIN : 2.0V/div, EN : 2.0V/div, VTT : 500mV/div, Time : 10ms/div

Start Up by EN



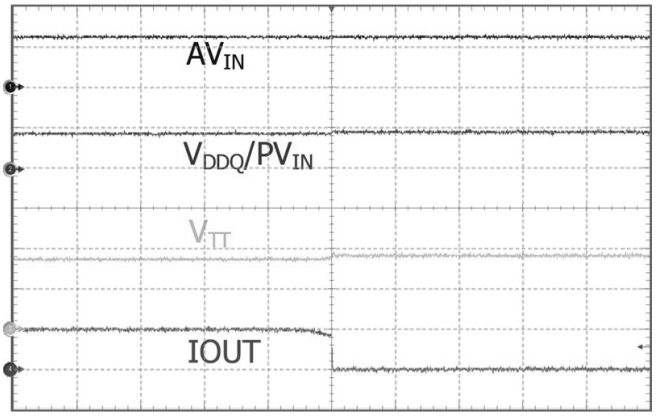
AVIN : 2.0V/div, VDDQ/PVIN : 2.0V/div, EN : 2.0V/div, VTT : 500mV/div, Time : 10ms/div

Shut Down by EN



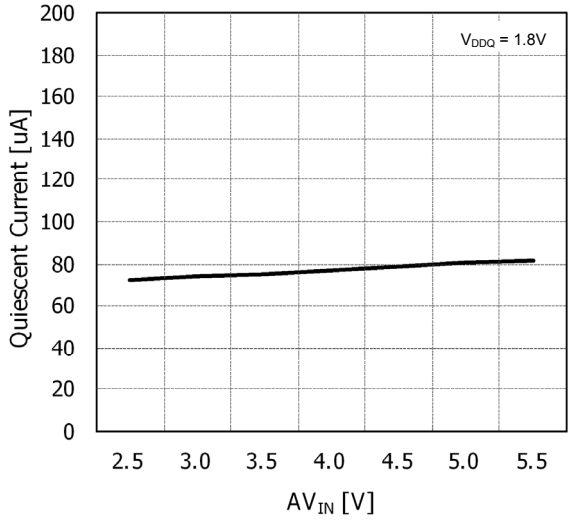
AVIN : 2.0V/div, VDDQ/PVIN : 2.0V/div, VTT : 500mV/div, IOUT : 1A/div, Time : 10ms/div

Load (0A → 1A)



AVIN : 2.0V/div, VDDQ/PVIN : 2.0V/div, VTT : 500mV/div, IOUT : 1A/div, Time : 10ms/div

Load (1A → 0A)



AV_{IN} vs. Quiescent Current

DESCRIPTION

The TJ2996 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2. The output, V_{TT} is capable of sinking and sourcing current while regulating the output voltage equal to V_{DDQ} / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The TJ2996 also incorporates two distinct power rails that separate the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the TJ2996 to provide a termination solution for the next generation of DDR-SDRAM memory (DDRII). The TJ2996 can also be used to provide a termination voltage for other logic schemes such as SSTL-3 or HSTL.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one R_S series resistor from the chipset to the memory and one R_T termination resistor. Typical values for R_S and R_T are 25 Ohms, although these can be changed to scale the current requirements from the TJ2996. This implementation can be seen below in Figure 1.

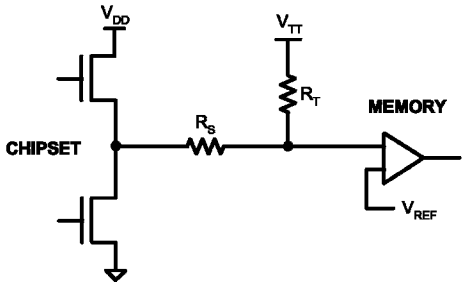


FIGURE 1. SSTL-Termination Scheme

PIN DESCRIPTION

AV_{IN} AND PV_{IN}

AV_{IN} and PV_{IN} are the input supply pins for the TJ2996. AV_{IN} is used to supply all the internal control circuitry. PV_{IN}, however, is used exclusively to provide the rail voltage for the output stage used to create V_{TT}. These pins have the capability to work off separate supplies depending on the application. Higher voltages on PV_{IN} will increase the maximum continuous output current because of output R_{DSON} limitations at voltages close to V_{TT}. The disadvantage of high values of PVIN is that the internal power loss will also increase, thermally limiting the design. For SSTL-2 applications, a good compromise would be to connect the AV_{IN} and PV_{IN} directly together at 2.5V. This eliminates the need for bypassing the two supply pins separately. The only limitation on input voltage selection is that PV_{IN} must be equal to or lower than AV_{IN}. It is recommended to connect PV_{IN} to voltage rails equal to or less than 3.3V to prevent the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown than the part will enter a shutdown state identical to the manual shutdown where V_{TT} is tri-stated and V_{REF} remains active.

V_{DDQ}

V_{DDQ} is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This guarantees that V_{TT} will track V_{DDQ} / 2 precisely. The optimal implementation of V_{DDQ} is as a remote sense. This can be achieved by connecting V_{DDQ} directly to the 2.5V rail at the DIMM instead of AV_{IN} and PV_{IN}. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications V_{DDQ} will be a 2.5V signal, which will create a 1.25V termination voltage at V_{TT} (See Electrical Characteristics Table for exact values of V_{TT} over temperature)

V_{SENSE}

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the TJ2996 then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the V_{SENSE} pin must still be connected to V_{TT}. Care should be taken when a long V_{SENSE} trace is implemented in close proximity to the memory. Noise pickup in the V_{SENSE} trace can cause problems with precise regulation of V_{TT}. A small 0.1uF ceramic capacitor placed next to the V_{SENSE} pin can help filter any high frequency signals and preventing errors.

SHUTDOWN

The TJ2996 contains an active low shutdown pin that can be used to tri-state V_{TT}. During shutdown V_{TT} should not be exposed to voltages that exceed AVIN. With the shutdown pin asserted low the quiescent current of the TJ2996 will drop, however, V_{DDQ} will always maintain its constant impedance of 100kΩ for generating the internal reference. Therefore to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the Thermal Dissipation section.

V_{REF}

V_{REF} provides the buffered output of the internal reference voltage V_{DDQ} / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically extremely high impedance, there should be little current drawn from V_{REF}. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 µF to 0.01 µF is recommended. This output remains active during the shutdown state for the suspend to RAM functionality.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to V_{DDQ} / 2. The TJ2996 is designed to handle peak transient currents of up to ± 3A with a fast transient response. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the TJ2996 is designed to handle large transient output currents it is not capable of handling these for long durations,

under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used (please refer to the Thermal Dissipation section). If the junction temperature exceeds the thermal shutdown point than V_{TT} will tri-state until the part returns below the hysteretic trip-point.

THERMAL DISSIPATION

Since the TJ2996 is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise, T_{Rmax} can be calculated given the maximum ambient temperature, T_{Amax} of the application and the maximum allowable junction temperature, T_{Jmax}.

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

From this equation, the maximum allowable power dissipation, P_{Dmax} of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA}$$

The maximum allowable value for junction-to-ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D = (T_{Jmax} - T_{Amax}) / P_D$$

The θ_{JA} of the TJ2996 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the θ_{JA} of the SOP8 is 165°C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 152°C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard.

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the Θ_{JA} further than the nominal values. Additional improvements in lowering the θ_{JA} can also be achieved with a constant airflow across the package.

Optimizing the θ_{JA} and placing the TJ2996 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at V_{TT}, either sinking or sourcing, and quiescent current at AVIN and V_{DDQ}. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$

Where, $P_{AVIN} = I_{AVIN} \times V_{AVIN}$

$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$

To calculate the maximum power dissipation at V_{TT} both conditions at V_{TT} need to be examined, sinking and sourcing current. Although only one equation will add into the total, V_{TT} cannot source and sink current simultaneously.

$P_{VTT} = V_{VTT} \times I_{LOAD}$ (Sinking) or $P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD}$ (Sourcing)

The power dissipation of the TJ2996 can also be calculated during the shutdown state. During this condition the output V_{TT} will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AV_{IN} and the constant impedance that is seen at the V_{DDQ} pin.

$P_D = P_{AVIN} + P_{VDDQ}$,

Where, $P_{AVIN} = I_{AVIN} \times V_{AVIN}$

$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$

TYPICAL APPLICATION INFORMATION

Several different application circuits have been shown in Figure 2 through Figure 11 to illustrate some of the options that are possible in configuring the TJ2996.

SSTL-2 APPLICATIONS

For the majority of applications that implement the SSTL-2 termination scheme it is recommended to connect all the input rails to the 2.5V rail. This provides an optimal trade-off between power dissipation and component count and selection. An example of this circuit can be seen in Figure 2.

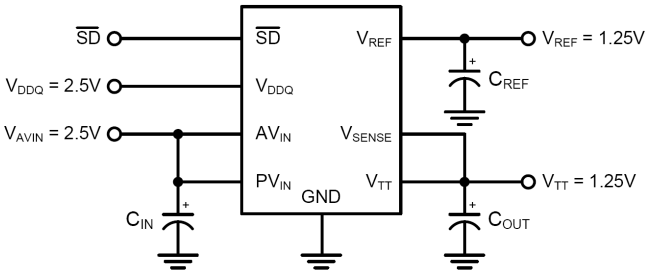


FIGURE 2. Recommended SSTL-2 Implementation

If power dissipation or efficiency is a major concern then the TJ2996 has the ability to operate on split power rails. The output stage (PV_{IN}) can be operated on a lower rail such as 1.8V and the analog circuitry (AV_{IN}) can be connected to a higher rail such as 2.5V, 3.3V or 5V. This allows the internal power dissipation to be lowered when sourcing current from V_{TT}. The disadvantage of this circuit is that the maximum continuous current is reduced because of the lower rail voltage, although it is adequate for all motherboard SSTL-2 applications. Increasing the output capacitance can also help if periods of large load transients will be encountered.

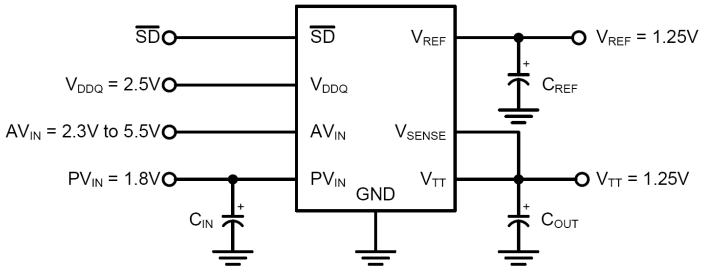


FIGURE 3. Lower Power Dissipation SSTL-2 Implementation

The third option for SSTL-2 applications in the situation that a 1.8V rail is not available and it is not desirable to use 2.5V is to connect the TJ2996 power rail to 3.3V. In this situation AV_{IN} will be limited to operation on the 3.3V or 5V rail as PV_{IN} can never exceed AV_{IN}. This configuration has the ability to provide the maximum continuous output current at the downside of higher thermal dissipation. Care should be taken to prevent the TJ2996 from experiencing large current levels which cause the junction temperature to exceed the maximum. Because of this risk it is not recommended to supply the output stage with a voltage higher than a nominal 3.3V rail.

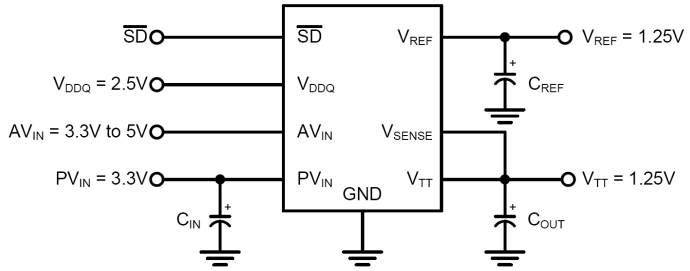


FIGURE 4. SSTL-2 Implementation with higher voltage rails

DDR-II APPLICATIONS

With the separate V_{DDQ} pin and an internal resistor divider it is possible to use the TJ2996 in applications utilizing DDR-II memory. Figure 3 and Figure 4 show several implementations of recommended circuits. Figure 3 shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8V rail and the AV_{IN} pin can be connected to either a 3.3V or 5V rail.

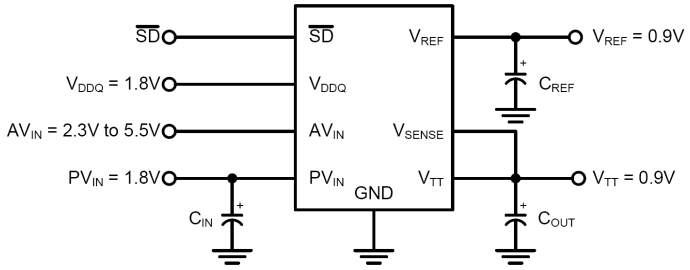


FIGURE 5. Recommended DDR-II Termination

If it is not desirable to use the 1.8V rail it is possible to connect the output stage to a 3.3V rail. Care should be taken to do not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages. For this reason it is not recommended to power PV_{IN} off a rail higher than the nominal 3.3V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

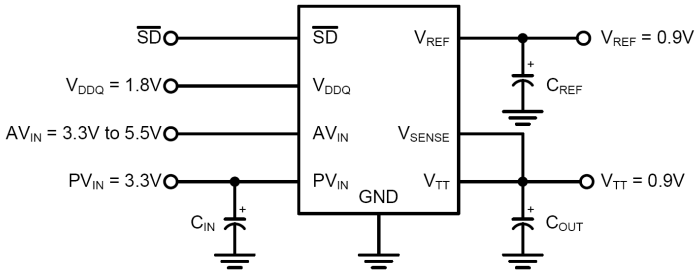


FIGURE 6. DDR-II Termination with higher voltage rails

LEVEL SHIFTING

If standards other than SSTL-2 are required, such as SSTL-3, it may be necessary to use a different scaling factor than 0.5 times V_{DDQ} for regulating the output voltage. Several options are available to scale the output to any voltage required. One method is to level shift the output by using feedback resistors from V_{TT} to the V_{SENSE} pin. This has been illustrated in Figures 7 and 8. Figure 7 shows how to use two resistors to level shift V_{TT} above the internal reference voltage of V_{DDQ} / 2. To calculate the exact voltage at V_{TT} the following equation can be used

$$V_{TT} = V_{DDQ} / 2 (1 + R1 / R2)$$

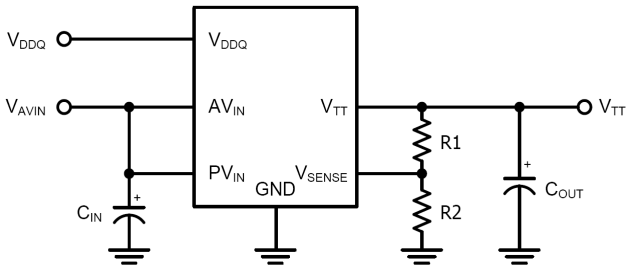


FIGURE 7. Increasing VTT by Level Shifting

Conversely, the R2 resistor can be placed between V_{SENSE} and V_{DDQ} to shift the V_{TT} output lower than the internal reference voltage of V_{DDQ} / 2. The equations relating V_{TT} and the resistors can be seen below:

$$V_{TT} = V_{DDQ} / 2 (1 - R1 / R2)$$

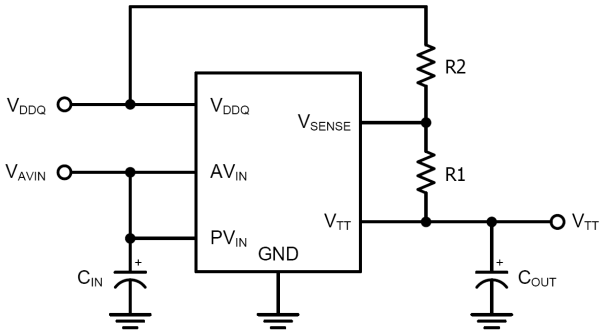


FIGURE 8. Decreasing VTT by Level Shifting

HSTL APPLICATIONS

The TJ2996 can be easily adapted for HSTL applications by connecting V_{DDQ} to the 1.5V rail. This will produce a V_{TT} and V_{REF} voltage of approximately 0.75V for the termination resistors. It is possible to connect PV_{IN} to higher than a 2.5V rail. Care should be taken to do not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages (For more information, refer to the Thermal Dissipation section.). The advantage of this configuration is that it has the ability to

source and sink a higher maximum continuous current. PV_{IN} can be also connected to a 1.8V rail and it has a limitation of maximum continuous current. PV_{IN} should be connected to a voltage higher than a 1.5V rail.

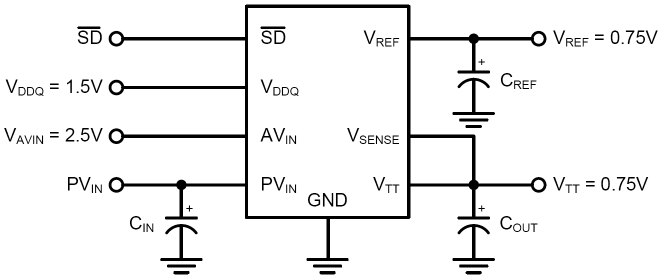


FIGURE 9. HSTL Application

QDR APPLICATIONS

Quad data rate (QDR) applications utilize multiple channels for improved memory performance. However, this increase in bus lines has the effect of increasing the current levels required for termination. The recommended approach in terminating multiple channels is to use a dedicated TJ2996 for each channel. This simplifies layout and reduces the internal power dissipation for each regulator. Separate V_{REF} signals can be used for each DIMM bank from the corresponding regulator with the chipset reference provided by a local resistor divider or one of the TJ2996 signals. Because V_{REF} and V_{TT} are expected to track and the part to part variations are minor, there should be little difference between the reference signals of each TJ2996.

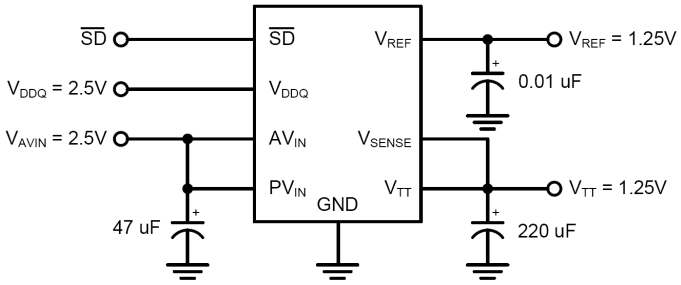


FIGURE 10. Typical SSTL-2 Application Circuit

OUTPUT CAPACITOR SELECTION

For applications utilizing the TJ2996 to terminate SSTL-2 I/O signals the typical application circuit shown in Figure 8 can be implemented. This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where V_{TT} is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. Figure 9 shown below depicts an example circuit where 2 bulk output capacitors could be situated at both ends of the V_{TT} plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

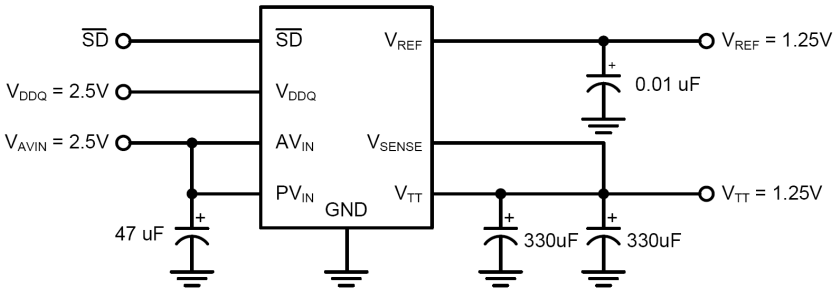


FIGURE 11. Typical SSTL-2 Application Circuit for Motherboards

In most PC applications an extensive amount of decoupling is required because of the long interconnects encountered with the DDR-SDRAM DIMMs mounted on modules. As a result bulk aluminum electrolytic capacitors in the range of 1000uF are typically used.

PCB LAYOUT CONSIDERATIONS

1. The input capacitor for the power rail should be placed as close as possible to the PV_{IN} pin.
2. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For mother- board applications an ideal location would be at the center of the termination bus.
3. V_{DDQ} can be connected remotely to the V_{DDQ} rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the V_{SENSE} trace to avoid noise pickup from switching I/O signals. A 0.1uF ceramic capacitor located close to the SENSE can also be used to filter any unwanted high frequency signal. This can be an issue especially if long SENSE traces are used.
6. V_{REF} should be bypassed with a 0.01µF or 0.1µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the V_{REF} pin